Attorney Docket No. 5308-376 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Meadows
Serial No.: 10/734,398
Filed: December 12, 2003
For: NON-UNIFORM GATE PITCH SEMICONDUCTOR DEVICES

Confirmation No. 1180
Group Art Unit: 2814
Examiner: Douglas A. Wille

Declaration of Ronald Meadows Under 37 C.F.R. § 1.131

Sir:

I, Ronald C. Meadows, hereby declare as follows:

1. I am the named inventor on U.S. Patent Application Serial No. 10/734,398 entitled, "Non-Uniform Gate Pitch Semiconductor Devices" (*hereinafter*, "the '398 application"), filed December 12, 2003.

2. From November 8, 1999 to May 14, 2005, I was employed as a Design Engineer at Cree, Inc., the assignee of the '398 application, located in Durham, N.C. My job responsibilities included the design of wide bandgap RF semiconductor devices.

3. I invented the subject matter of the '398 application. In particular, I conceived and reduced to practice the subject matter of the '398 application in the United States prior to November 2, 2001.

4. Prior to November 2, 2001, I designed and caused to be fabricated 3 lots, including a total of 16 completed wafers corresponding to 1248 dice, of 30W SiC MESFET devices ("30W devices") having a non-uniform gate structure in an effort to create transistors having lower peak junction temperatures and/or more uniform junction temperatures during RF operation. Each of the 30W devices included 36 unit cells connected in parallel. Each unit cell included a source region and a drain region. The 30W devices each included a plurality of gate fingers electrically connected in parallel.

5. Prior to fabricating the 30W devices, a thermal simulation of the 30W devices was performed at Cree using Harvard Thermal, Inc. TAS thermal modeling software. The results of the thermal simulation, which are shown in Figure 3 of the '398 application, predicted lower peak junction temperatures and more uniform junction temperatures during RF operation for the 30W devices.

6. The spacing of the gate fingers of the unit cells of the 30W devices decreased outwards in a pseudo-linear fashion from a large pitch at the innermost gate fingers to a small pitch at the outermost fingers. The spacing of the central pairs of gate fingers in the 30W devices was approximately 100.5 μm. The spacing of the outermost pairs of gate fingers in the 30W devices was approximately 59.5 μm. Thus, for half the device, gate pitches of 100.5, 90, 90.5, 85, 90.5, 89.5, 90.5, 85, 90.5, 84.5, 80.5, 79.5, 80.5, 75, 75, 65, 55, and 59.5 μm were utilized.

7. I also designed and caused to be fabricated, on the same wafers as the 30W SiC MESFET devices, 1248 dice of 60W SiC MESFET devices("60W devices") having a non-uniform gate pitch design. The 60W devices were designed and fabricated prior to November 2, 2001. Each of the fabricated 60W devices included 48 unit cells connected in parallel. Each unit cell included a source region and a drain region. The 60W devices each included a plurality of gate fingers electrically connected in parallel.

8. The spacing of the gate fingers of the unit cells of the 60W devices decreased outwards in a pseudo-linear fashion from a large pitch at the innermost fingers to a small pitch at the outermost gate fingers. The spacing of the innermost pairs of gate fingers in the 60W devices was 100.5 μm. The spacing of the outermost pairs of gate fingers in the 60W devices was approximately 55 μm. Thus, for half the device, gate pitches of 100.5, 85, 87.5, 92.5, 90.5, 89.5, 80, 79.5, 80.5, 80, 90, 99.5, 90, 80, 80.5, 79.5, 80.5, 79.5, 80.5, 60, 60, 67.5, 62.5, and 55 μm were utilized.

9. A CAD device layout for the 30W and 60W SiC MESFET devices having non-uniform gate structures is attached hereto as Exhibit A. I designed the CAD layout shown in Exhibit A prior to November 2, 2001. The layout of the 30W SiC MESFET device having a non-uniform gate structure is identified in Exhibit A as device A-30. The layout of the 60W SiC MESFET device having a non-uniform gate structure is identified in Exhibit A as device A-60. The 30W and 60W devices were fabricated on the same wafers using the same mask set.

10. Within the same mask layout shown in Exhibit A, a 30W SiC MESFET device and a 60W SiC MESFET device having uniform gate pitches were included for comparison purposes. The layout of the 30W SiC MESFET device having a uniform gate pitch is identified in Exhibit A as device B-30. The layout of the 60W SiC MESFET device having a uniform gate pitch is identified in Exhibit A as device B-60. Devices B-30 and B-60 each had a fixed gate pitch of 80 μm. A 10-W test cell, identified as device B-10, was also included in the layout.

11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Ronald C. Meadows

Ronald C. Meadows

2/28/06

Date